<u>REMARKS</u>

Claims 8, 16, 22 and 24 have been amended to remove indefinite features therein previously inadvertently not amended. Claims 1 to 30 remain active in this application.

Claims 1 to 17 were rejected under 35 U.S.C 103(a) as being unpatentable ove Lin et al. (U.S. 6,297,082) in view of Nakahara (U.S. 5,075,242). The rejection is respectfully traversed.

The invention relates to semiconductor device fabrication, wherein source/drain regions in one transistor are implanted using a threshold voltage (VT) adjust implantation, which is <u>concurrently</u> also being used to adjust the threshold voltage of another transistor. Using this technique, the source/drain regions of high voltage MOSFET devices can be implanted <u>while</u> adjusting the threshold voltage of lower voltage MOSFETS. Thus, the somewhat lower dosage implant can <u>simultaneously or contemporaneously</u> be used to implant the channel (*e.g.*, or indeed the entire active area) associated with a low voltage device, along with the source/drain regions of a higher voltage device, for example, using appropriate VT adjust implantation masking. The high voltage device source/drain regions can then be masked from subsequent LDD implantation of the low voltage device source/drain regions. As a result, the appropriate [illegible] <u>adding extra processing steps</u>. Thus, the invention can be advantageously employed in split gate oxide device processing to control CHC degradation without adversely impacting product cost by minimizing the steps required in processing.

In this regard, claim 1 requires the step of implanting a first transistor region associated with a first transistor device in the semiconductor device substrate to adjust a

threshold voltage associated with the first transistor device and concurrently implanting a portion of a second transistor region in the semiconductor device substrate associated with a second transistor device in the semiconductor device to form source/drain regions associated with the second transistor device with a channel region between the source/drain regions. No such step is taught or suggested by Lin et al. Note in Figs. 2A to 2F of Lin et al., the figures referred to in the Office action, that no concurrence as required. Note that each of the transistors is formed individually and all of the transistors are formed after formation of the two level gate oxide.

Claim 1 further requires the step of then forming a first gate oxide structure overlying a channel region in the first transistor region, the first gate oxide structure having a first thickness and forming a second gate oxide structure overlying the channel region in the second transistor region, the second gate oxide structure having a second thickness, the second thickness being greater than the first thickness. No such step is taught or suggested by Lin et al. There is no channel in Lin et al. when the gate oxide is formed. Furthermore, as noted above, the gate oxide of Lin et al. is formed prior to formation of the source/drain regions of any of the implants as required by the claim.

With reference to Nakahara, this reference, this reference fails to overcome the

In proceedings before the Patent and Trademark Office, "the Examiner bears the burden of establishing a prima facie case of obviousness based upon the prior art". In re Fritch, 23 USPQ2d 1780, 1783 (Fed. Cir. 1992) (citing In re Piasecki, 745 F.2d 1468, 1471-72, 223 USPQ 785, 787-88 (Fed. Cir. 1984). "The Examiner can satisfy this burden only by showing some objective teaching in the prior art or that knowledge generally available to

one of ordinary skill in the art would lead that individual to combine the relevant teachings of the references", In re Fritch, 23 USPQ2d 1780, 1783 (Fed. Cir. 1992)(citing In re Fine, 837 F.2d 1071, 1074, 5 USPQ2d 1596, 1598 (Fed. Cir. 1988)(citing In re Lalu, 747 F.2d 703, 705, 223 USPQ 1257, 1258 (Fed. Cir. 1988)). Thus, the burden is on the Examiner to present a prima facie case of obviousness of the claims – the initial burden is not on Appellants to prove that their claims are non-obvious. Statements that "one of ordinary skill in the art of making semiconductor devices" without more does not meet this burden.

To establish a prima facie case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest ALL the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure. In re Vaeck, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991). In the present case, the first requirement of In re Vaeck has not been met since

themselves or in the knowledge generally available to one of ordinary skill in the art as demonstrated in the record, to modify the combined reference teachings of Lin et al and Nakahara to include the elements discusses above as to claim 1. The second requirement of In re Vaeck has not been met since there is NO reasonable expectation of success that the combination of Lin et al. and Nakahara will accomplish what the Examiner and states the

combination will accomplish. The third requirement of <u>In re Vaeck</u> has similarly not been met since the Lin et al and Nakahara references themselves do NOT teach or suggest ALL the claim limitations.

Claims 2 to 17 depend from claim 1 and therefore define patentably over the applied references for at least the reasons set forth above with reference to claim 1.

In addition, claim 2 further limits claim 1 by requiring the step of <u>then</u> implanting a portion of the first transistor region to form source/drain regions associated with the first transistor device. This step requires additional implantation into the first transistor region as a further part of the improved procedure of the present invention. No such step is taught or suggested by Lin et al., Nakahara or any proper combination of these references.

Claim 3 further limits claim 2 by further requiring the steps of then implanting a third transistor region associated with a third transistor device in the semiconductor device using a third implantation process to adjust a threshold voltage associated with the third transistor device and concurrently implanting a portion of a fourth transistor region in the semiconductor device substrate associated with a fourth transistor device in the semiconductor device to form source/drain regions associated with the fourth transistor

gate oxide structure overlying a channel region in the third transistor region, the third gate oxide structure having a third thickness and forming a fourth gate oxide structure overlying the channel region in the fourth transistor region, the fourth gate oxide structure having a fourth thickness, the fourth thickness being greater than the third thickness. No such steps are taught or suggested by Lin et al., Nakahara or any proper combination of

these references. Again, the order and concurrency of the steps is important and not taught or suggested by the applied references.

Claim 4 further limits claim 3 by further requiring the step of implanting a portion of the third transistor region to form a source/drain region associated with the third transistor device. This step requires additional implantation into the third transistor region as a further part of the improved procedure of the present invention. No such step is taught or suggested by Lin et al., Nakahara or any proper combination of these references in the combination as claimed.

Claim 5 further limits claim 3 by requiring that the first and third transistor devices include a first one of an NMOS transistor and a PMOS transistor, and that the second and fourth transistor devices comprise a second one of an NMOS transistor and a PMOS transistor. No such step is taught or suggested by Lin et al., Nakahara or any proper combination of these references in the combination as claimed.

Claim 6 further limits claim 3 by requiring that the first and third transistor devices include NMOS transistors and the second and fourth transistor devices comprise PMOS transistors and implanting the third transistor region and a portion of the fourth transistor region includes implanting phosphorus in the third transistor region and a [illegible] Nakahara or any proper combination of these references in the combination as claimed.

Claim 7 further limits claim 6 by requiring that the step of implanting phosphorus in the third transistor region and a portion of the fourth transistor region include the steps of performing a phosphorus threshold adjustment implantation in the third transistor region and a portion of the fourth transistor region using a dose of about 8 E11 cm^{-2} and

an energy of about 20 keV and performing a phosphorus punch-through implantation in the third transistor region and a portion of the fourth transistor region using a dose of about 2 E12 cm^{-2} and an energy of about 70 keV. No such steps are taught or suggested by Lin et al., Nakahara or any proper combination of these references in the combination as claimed.

Claim 8 further limits claim 4 by requiring that the first and third transistor devices comprise NMOS transistors and the second and fourth transistor devices comprise PMOS transistors and implanting a portion of the third transistor region includes implanting boron in a portion of the fourth transistor region. No such step is taught or suggested by Lin et al., Nakahara or any proper combination of these references in the combination as claimed.

Claim 9 further limits claim 8 by requiring that the step of implanting boron in a portion of the fourth transistor region include performing a boron LDD implantation in a portion of the fourth transistor region using a dose of about 4 E13 cm^{-2} and an energy of about 20 keV. No such step is taught or suggested by Lin et al., Nakahara or any proper combination of these references either alone or in the combination as claimed.

Claim 10 further limits claim 2 by requiring that the first transistor device include

step of implanting a portion of the first transistor region includes implanting at least one of phosphorus and arsenic in a portion of the first transistor region. No such step is taught or suggested by Lin et al., Nakahara or any proper combination of these references in the combination as claimed.

Claim 11 further limits claim 10 by requiring that the step of implanting at least one of phosphorus and arsenic in a portion of the first transistor region include performing a phosphorus LDD implantation in a portion of the first transistor region using a dose of about 4 E13 cm^{-2} and an energy of about 40 keV. No such step is taught or suggested by Lin et al., Nakahara or any proper combination of these references either alone or in the combination as claimed.

Claim 12 further limits claim 1 by requiring that the first transistor device include an NMOS transistor, the second transistor device including a PMOS transistor, and the step of implanting the first transistor region and a portion of the second transistor region include implanting boron in the first transistor region and a portion of the second transistor region. No such step is taught or suggested by Lin et al., Nakahara or any proper combination of these references in the combination as claimed.

Claim 13 further limits claim 12 by requiring that the step of implanting boron in the first transistor region and a portion of the second transistor region include the steps of performing a boron threshold adjustment implantation in the first transistor region and a portion of the second transistor region using a dose of about 3 E12 cm^{-2} and an energy of about 20 keV and performing a boron punch-through implantation in the first transistor [illegible] an energy of about 70 keV. No such steps are taught or suggested by Lin et al., Nakahara or any proper combination of these references in the combination as claimed.

Claim 14 further limits claim 1 by requiring that the first thickness be about 65 Å or more and the second thickness be about 300 Å or less. No such step is taught or

suggested by Lin et al., Nakahara or any proper combination of these references in the combination as claimed.

Claim 15 further limits claim 14 by requiring that the first thickness be about 75 Å and the second thickness be about 200 Å. No such step is taught or suggested by Lin et al., Nakahara or any proper combination of these references in the combination as claimed.

Claim 16 further limits claim 1 by requiring that the first transistor device comprises a PMOS transistor, wherein the second transistor device comprises an NMOS transistor, and wherein implanting the first transistor region and a portion of the second transistor region comprises implanting phosphorus in the first transistor region and a portion of the second transistor region. No such step is taught or suggested by Lin et al., Nakahara or any proper combination of these references in the combination as claimed

Claim 17 further limits claim 16 by requiring that the step of implanting phosphorus in the first transistor region and a portion of the second transistor region include the steps of performing a phosphorus threshold adjustment implantation in the first transistor region and a portion of the second transistor region using a dose of about 8 E11 cm^{-2} and an energy of about 20 keV and performing a phosphorus punch-through

using a dose of about 2 E12 cm^{-2} and an energy of about 70 keV. No such step is taught or suggested by Lin et al., Nakahara or any proper combination of these references

Claims 18 to 25 were rejected under 35 U.S.C. 103(a) as being unpatentable over Lin et al. The rejection is respectfully traversed.

The argument presented above with reference to claim 1 is incorporated by reference as to claim 18.

More specifically, claim 18 requires the step adjusting a threshold voltage of a first transistor device in a first region of said semiconductor device substrate while concurrently forming a source/drain region of a second transistor device, both using the same implant. As discussed above, this concurrency is not found in Lin et al.

Claims 19 to 25 depend from claim 18 and therefore define patentably over the applied references for at least the reason set forth above as to claim 18.

Claim 19 further limits claim 18 by requiring the step of forming a source/drain region of the first transistor device. No such step is taught or suggested by Lin et al., Nakahara or any proper combination of these references

Claim 20 further limits claim 19 by further requiring the steps of then forming a first gate oxide structure of the first transistor device having a first thickness and forming a second gate oxide structure of the second transistor device having a second thickness, the second thickness being greater than the first thickness. No such step is taught or suggested by Lin et al., Nakahara or any proper combination of these references either alone or in the combination as claimed.

threshold voltage of a third transistor device and forming a source/drain region of a fourth transistor device. No such step is taught or suggested by Lin et al., Nakahara or any proper combination of these references either alone or in the combination as claimed.

Claim 22 further limits claim 21 by requiring the steps of forming a source/drain region of the third transistor device. No such step is taught or suggested by Lin et al., Nakahara or any proper combination of these references in the combination as claimed.

Claim 23 further limits claim 22 by requiring that the first and third transistor devices include a first one of NMOS transistors and PMOS transistors and the second and fourth transistors include a second one of NMOS transistors and PMOS transistors. No such step is taught or suggested by Lin et al., Nakahara or any proper combination of these references in the combination as claimed.

Claim 24 further limits claim 18 by requiring that the first transistor device include an NMOS transistor, the second transistor device include a PMOS transistor and the step of adjusting a threshold voltage of the first transistor device and forming a source/drain region of the second transistor device include selectively implanting a first transistor region associated with the first transistor device to adjust a threshold voltage associated with the first transistor device and implanting a portion of a second transistor region associated with the second transistor device to form a source/drain region associated with the second transistor device using boron. No such step is taught or suggested by Lin et al., Nakahara or any proper combination of these references either

Claim 25 further limits claim 18 by requiring that the first transistor device include a PMOS transistor, the second transistor device include an NMOS transistor and the step of adjusting a threshold voltage of the first transistor device and forming a source/drain region of the second transistor device includes selectively implanting a first transistor region associated with the first transistor device to adjust a threshold voltage

associated with the first transistor device and implanting a portion of a second transistor region associated with the second transistor device to form a source/drain region associated with the second transistor device using phosphorus. No such step is taught or suggested by Lin et al., Nakahara or any proper combination of these references either alone or in the combination as claimed.

Claims 26 and 27 were rejected under 35 U.S.C. 103(a) as being unpatentable over Lin et al. in view of Nakahara. The rejection is respectfully traversed.

The argument presented above with reference to claim 1 is incorporated herein by reference.

More specifically, claim 26 requires the step of selectively concurrently implanting a first transistor region in the semiconductor device substrate to adjust a threshold voltage associated with a first transistor device and a portion of a second transistor region to form a source/drain region associated with a second transistor device. No such step is taught or suggested by Lin et al., Nakahara or any proper combination of these references either alone or in the combination as claimed.

Claim 27 depends from claim 26 and therefore defines patentably over the applied references for at least the reason stated above with reference to claim 26.

selectively implanting the first transistor region and a portion of the second transistor region include the step of implanting one of phosphorus, arsenic and boron in the first transistor region and a portion of the second transistor region. No such step is taught or suggested by Lin et al., Nakahara or any proper combination of these references in the combination as claimed.

Claims 28 to 30 were rejected under 35 U.S.C. 103(a) as being unpatentable over Lin et al. in view of Nakahara. The rejection is respectfully traversed.

The argument presented above with reference to claim 1 is incorporated herein by reference.

More specifically, claim 28 requires the step of concurrently implanting in the semiconductor device substrate an active region of a low voltage NMOS device and source/drain regions of a high voltage PMOS device using a boron threshold voltage adjust implantation. No such step is taught or suggested by Lin et al., Nakahara or any proper combination of these references either alone or in the combination as claimed.

Claim 28 further requires the step of implanting an active region of a low voltage PMOS device and source/drain regions of a high voltage NMOS device using a phosphorus threshold voltage adjust implantation process. No such step is taught or suggested by Lin et al., Nakahara or any proper combination of these references either alone or in the combination as claimed.

Claim 28 still further requires the step of forming polysilicon gate structures associated with the high and low voltage NMOS and PMOS devices. No such step is taught or suggested by Lin et al., Nakahara or any proper combination of these references

Claim 28 yet further requires the step of implanting source/drain regions associated with the low voltage NMOS device using a phosphorus or arsenic LDD implantation. No such step is taught or suggested by Lin et al., Nakahara or any proper combination of these references in the combination as claimed.

Claim 28 even further requires the step of implanting source/drain regions associated with the low voltage PMOS device using a boron LDD implantation. No such step is taught or suggested by Lin et al., Nakahara or any proper combination of these references in the combination as claimed.

Claims 29 and 30 depend from claim 28 and therefore define patentably over the applied references for at least the reason presented above with reference to claim 28.

Claim 29 further limits claim 28 by requiring the steps of forming sidewall spacers on opposite sides of the polysilicon gate structures, further implanting the source/drain regions associated with the low and high voltage NMOS devices using a phosphorus or arsenic implantation and further implanting the source/drain regions associated with the low and high voltage PMOS devices using a boron implantation. No such step is taught or suggested by Lin et al., Nakahara or any proper combination of these references either alone or in the combination as claimed.

Claim 30 further limits claim 29 by requiring that the steps of forming a first gate oxide layer having a first thickness overlying the active regions associated with the low voltage NMOS and PMOS devices and forming a second gate oxide layer having a second thickness overlying the active regions associated with high voltage NMOS and

step is taught or suggested by Lin et al., Nakahara or any proper combination of these references either alone or in the combination as claimed.

In view of the above remarks, favorable reconsideration and allowance are respectfully requested.

Respectfully submitted,

Jay M. Cantor
Reg. No. 19906
(202) 639-7713

1. A method of fabricating MOSFET transistors in a semiconductor device, comprising the steps of:

providing a semiconductor device substrate;

implanting a first transistor region associated with a first transistor device in the semiconductor device substrate to adjust a threshold voltage associated with the first transistor device and concurrently implanting a portion of a second transistor region in the semiconductor device substrate associated with a second transistor device in the semiconductor device to form source/drain regions associated with the second transistor device with a channel region between said source/drain regions;

then forming a first gate oxide structure overlying a channel region in the first transistor region, the first gate oxide structure having a first thickness and forming a second gate oxide structure overlying the channel region in the second transistor region, the second gate oxide structure having a second thickness, the second thickness being greater than the first thickness.

2. The method of claim 1, further comprising the step of then implanting a portion of the first transistor region to form source/drain regions associated with the first transistor device.

3. The method of claim 2, further comprising the steps of then implanting a

device using a third implantation process to adjust a threshold voltage associated with the third transistor device and concurrently implanting a portion of a fourth transistor region in the semiconductor device substrate associated with a fourth transistor device in the semiconductor device to form source/drain regions associated with the fourth transistor device with a channel region between said source/drain regions;

then forming a third gate oxide structure overlying a channel region in the third transistor region, the third gate oxide structure having a third thickness and forming a

fourth gate oxide structure overlying the channel region in the fourth transistor region, the fourth gate oxide structure having a fourth thickness, the fourth thickness being greater than the third thickness.

4. The method of claim 3, further comprising the step of implanting a portion of the third transistor region to form a source/drain region associated with the third transistor device.

5. The method of claim 3, wherein the first and third transistor devices comprise a first one of an NMOS transistor and a PMOS transistor, and wherein the second and fourth transistor devices comprise a second one of an NMOS transistor and a PMOS transistor.

6. The method of claim 3, wherein the first and third transistor devices comprise NMOS transistors, wherein the second and fourth transistor devices comprise PMOS transistors, and wherein implanting the third transistor region and a portion of the fourth transistor region comprises implanting phosphorus in the third transistor region and a portion of the fourth transistor region.

7. The method of claim 6, wherein implanting phosphorus in the third transistor region and a portion of the fourth transistor region comprises the steps of:

performing a phosphorus threshold adjustment implantation in the third transistor region and a portion of the fourth transistor region using a dose of about 8 E11 cm^{-2} and an energy of about 20 keV; and

performing a phosphorus punch-through implantation in the third transistor region and a portion of the fourth transistor region using a dose of about 2 E12 cm^{-2} and an energy of about 70 keV.

8. The method of claim 4, wherein the first and third transistor devices comprise NMOS transistors, wherein the second and fourth transistor devices comprise

PMOS transistors, and wherein implanting a portion of the third transistor region comprises implanting boron in a portion of the fourth transistor region.

9. The method of claim 8, wherein implanting boron in a portion of the fourth transistor region comprises performing a boron LDD implantation in a portion of the fourth transistor region using a dose of about 4 E13 cm^{-2} and an energy of about 20 keV.

10. The method of claim 2, wherein the first transistor device comprises an NMOS transistor, wherein the second transistor device comprises a PMOS transistor, and wherein implanting a portion of the first transistor region comprises implanting at least one of phosphorus and arsenic in a portion of the first transistor region.

11. The method of claim 10, wherein implanting at least one of phosphorus and arsenic in a portion of the first transistor region comprises performing a phosphorus LDD implantation in a portion of the first transistor region using a dose of about 4 E13 cm^{-2} and an energy of about 40 keV.

12. The method of claim 1, wherein the first transistor device comprises an NMOS transistor, wherein the second transistor device comprises a PMOS transistor, and wherein implanting the first transistor region and a portion of the second transistor region comprises implanting boron in the first transistor region and a portion of the second transistor region.

13. The method of claim 12, wherein implanting boron in the first transistor region and a portion of the second transistor region comprises the steps of:

performing a boron threshold adjustment implantation in the first transistor region and a portion of the second transistor region using a dose of about 3 E12 cm^{-2} and an energy of about 20 keV; and

performing a boron punch-through implantation in the first transistor region and a portion of the second transistor region using a dose of about 4 E12 cm^{-2} and an energy of about 70 keV.

14. The method of claim 1, wherein the first thickness is about 65 Å or more and the second thickness is about 300 Å or less.

15. The method of claim 14, wherein the first thickness is about 75 Å and the second thickness is about 200 Å.

16. The method of claim 1, wherein the first transistor device comprises a PMOS transistor, wherein the second transistor device comprises an NMOS transistor, and wherein implanting the first transistor region and a portion of the second transistor region comprises implanting phosphorus in the first transistor region and a portion of the second transistor region.

17. The method of claim 16, wherein implanting phosphorus in the first transistor region and a portion of the second transistor region comprises the steps of:

performing a phosphorus threshold adjustment implantation in the first transistor region and a portion of the second transistor region using a dose of about 8 E11 cm^{-2} and an energy of about 20 keV; and

performing a phosphorus punch-through implantation in the first transistor region [illegible] transistor region using a dose of about 2 E12 cm^{-2} and an energy of about 70 keV.

18. A method of fabricating MOSFET transistors in a semiconductor device, comprising the steps of:

providing a semiconductor substrate;

adjusting a threshold voltage of a first transistor device in a first region of said semiconductor device substrate; and concurrently forming a source/drain region of a second transistor device, both using the same implant.

19. The method of claim 18, further comprising the step of forming a source/drain region of the first transistor device.

20. The method of claim 19, further comprising the steps of:

then forming a first gate oxide structure of the first transistor device having a first thickness; and

forming a second gate oxide structure of the second transistor device having a second thickness, the second thickness being greater than the first thickness.

21. The method of claim 19, further comprising the steps of then adjusting a threshold voltage of a third transistor device and forming a source/drain region of a fourth transistor device.

22. The method of claim 21, further comprising the steps of forming a source/drain region of the third transistor device.

23. The method of claim 22, wherein the first and third transistor devices comprise a first one of NMOS transistors and PMOS transistors, and wherein the second and fourth transistors comprise a second one of NMOS transistors and PMOS transistors.

24. The method of claim 18, wherein the first transistor device comprises an [illegible] device comprises a PMOS transistor, and wherein adjusting a threshold voltage of the first transistor device and [illegible] source/drain region of the second transistor device comprises selectively implanting a first transistor region associated with the first transistor device to adjust a threshold voltage associated with the first transistor device, and implanting a portion of a second transistor region associated with the second transistor device to form a source/drain region associated with the second transistor device using boron.

25. The method of claim 18, wherein the first transistor device comprises a PMOS transistor, wherein the second transistor device comprises an NMOS transistor, and wherein adjusting a threshold voltage of the first transistor device and forming a source/drain region of the second transistor device comprises selectively implanting a first transistor region associated with the first transistor device to adjust a threshold voltage associated with the first transistor device, and implanting a portion of a second transistor region associated with the second transistor device to form a source/drain region associated with the second transistor device using phosphorus.

26. A method of forming a source/drain region in a semiconductor device, comprising the steps of:

providing a semiconductor device substrate; and

selectively concurrently implanting a first transistor region in said semiconductor device substrate to adjust a threshold voltage associated with a first transistor device and a portion of a second transistor region to form a source/drain region associated with a second transistor device.

27. The method of claim 26, wherein selectively implanting the first transistor region and a portion of the second transistor region comprises the step of implanting one of phosphorus, arsenic and boron in the first transistor region and a portion of the second transistor region.

[illegible] semiconductor device, comprising the steps of

providing a semiconductor device substrate;

concurrently implanting in said semiconductor device substrate an active region of a low voltage NMOS device and source/drain regions of a high voltage PMOS device using a boron threshold voltage adjust implantation;

implanting an active region of a low voltage PMOS device and source/drain regions of a high voltage NMOS device using a phosphorus threshold voltage adjust implantation process;

forming polysilicon gate structures associated with the high and low voltage NMOS and PMOS devices;

implanting source/drain regions associated with the low voltage NMOS device using a phosphorus or arsenic LDD implantation; and

implanting source/drain regions associated with the low voltage PMOS device using a boron LDD implantation.

29. The method of claim 28, further comprising the steps of:

forming sidewall spacers on opposite sides of the polysilicon gate structures;

further implanting the source/drain regions associated with the low and high voltage NMOS devices using a phosphorus or arsenic implantation; and

further implanting the source/drain regions associated with the low and high voltage PMOS devices using a boron implantation.

30. The method of claim 29, further comprising the steps of:

forming a first gate oxide layer having a first thickness overlying the active regions associated with the low voltage NMOS and PMOS devices; and

forming a second gate oxide layer having a second thickness overlying the active regions associated with high voltage NMOS and PMOS devices, wherein the second thickness is greater than the first thickness.